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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte BRENT KEETH and PIERRE C. FAZAN

Appeal 2007-3528
Application 08/530,661
Technology Center 2800

Decided: May 14, 2008

Before JOSEPH F. RUGGIERO, ANITA PELLMAN GROSS,
and SCOTT R. BOALICK, *Administrative Patent Judges*.

RUGGIERO, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134 from the Final Rejection of claims 6-10, 18, 19, 22, 23, 25, and 26, which are all of the claims pending in this application. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

Appellants' invention relates to semiconductor memory fabrication at the 64M and 16M integration levels. The present claims on appeal are directed to a semiconductor memory device which, according to Appellants, is of a smaller size or consumed monolithic die area than prior art devices (Spec. 34-40).

Claim 6 is illustrative of the invention and reads as follows:

6. A semiconductor device including a memory, the semiconductor device comprising:

a semiconductor die encapsulated in a package, the package having an encapsulating body and electrically conductive interconnect pins extending outwardly from the body;

a total of from 16,000,000 to 17,000,000 functional and operably addressable memory cells arranged in multiple memory arrays formed on the die, the individual functional and operably addressable memory cells occupying area on the die within the memory arrays, the occupied area of all functional and addressable memory cells on the die having a total combined area which is no greater than 14 mm^2; and

peripheral circuitry and pitch circuitry formed on the die relative to the memory arrays; the peripheral circuitry electrically interconnecting with the pins and including operably interconnected control and timing circuitry, address and redundancy circuitry, data and test path circuitry, and voltage supply circuitry which collectively enable full access to all addressable memory cells of the memory arrays.

The Examiner relies on the following prior art references to show unpatentability:

Takahashi	US 5,287,000	Feb. 15, 1994
Eimori	US 5,610,418	Mar. 11, 1997 (filed Jun. 6, 1995)
Nakamura	US 5,654,577	Aug. 5, 1997 (filed Jun. 7, 1995)
Takashima	US 5,838,038	Nov. 17, 1998 (filed Jun. 7, 1995)

Claims 6-10, 18, 19, 22, 23, 25, and 26, all of the appealed claims, stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Takashima in view of Eimori, Nakamura, and Takahashi.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the Briefs and Answer for the respective details. Only those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants could have made but chose not to make in the Briefs have not been considered and are deemed to be waived [see 37 C.F.R. § 41.37(c)(1)(vii)].

ISSUE

Under 35 U.S.C § 103(a), with respect to appealed claims 6-10, 18, 19, 22, 23, 25, and 26, would one of ordinary skill in the art at the time of the invention have found it obvious to combine Takashima, Eimori, Nakamura, and Takahashi to render the claimed invention unpatentable?

PRINCIPLES OF LAW

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. *See In re Fine*, 837 F.2d 1071, 1073 (Fed. Cir. 1988). In so doing, the Examiner must make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). "[T]he examiner bears the initial burden, on review of the prior art or on any other ground, of presenting a *prima facie* case of unpatentability." *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). Furthermore,

> '. . .there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness' . . . [H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ. *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (2007)(quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

ANALYSIS

With respect to the Examiner's 35 U.S.C. § 103(a) rejection of appealed independent claim 6 based on the combination of Takashima, Eimori, Nakamura, and Takahashi, Appellants' arguments in response assert a failure to set forth a prima facie case of obviousness since all of the claimed limitations are not taught or suggested by the applied prior art references. Appellants' arguments (App. Br. 9-10; Reply Br. 4) initially focus on the contention that the Examiner's conclusion that applying the 0.25 μm design rule taught by Eimori to the $6F^2$ device size teachings of Takashima as modified by Nakamura and Takahashi would result in an occupied memory cell area of 6 mm^2 is based on a misapplication of the term

"design rule." According to Appellants (*id.*), since a "design rule" refers to a minimum feature size, i.e., the minimum feature size that can be etched, an actual device manufactured according to a 0.25 μm design rule will include features that have larger dimensions as evidenced by Figures 6 and 9 in Eimori. Therefore, Appellants contend, the occupied memory cell area in the device resulting from the Examiner's proposed combination of references will be larger than the 6 mm^2 size asserted by the Examiner.

We do not find Appellants' argument to be persuasive. We do agree with Appellants that a "design rule," i.e., the value of "F," refers to only a minimum feature size and that other features will perhaps be larger. While Appellants contend, therefore, that the area size of the device resulting from the Examiner's proposed combination will be larger than 6 mm^2, it is noteworthy that the recited memory cell size limitation in independent claim 6 encompasses a much larger area, i.e., "no greater than 14 mm^2." As pointed out by the Examiner (Ans. 5), while Eimori does show (Figure 6) a 0.35 μm feature size in addition to the 0.25 μm design rule feature size, the total area of the structure shown by Eimori's Figure 6 (0.6 μm x 0.95 μm = 0.57 μm^2) in 16M cell integration as claimed would be well within the "no greater than 14 mm^2" area size claimed requirement.

In a related argument, Appellants contend (App. Br. 9-10) that the Examiner's determined 6 mm^2 cell area size resulting from the application of Eimori's 0.25 μm design rule to Takashima's $6F^2$ device size structure is faulty because standard memory device fabrication actually includes a large number of redundant cells to replace inoperable memory cells. We would point out, however, that even assuming the correctness of Appellants' contention that sufficient area must be allotted on an integrated memory cell

device structure for redundant memory cells, no such redundant cell area structure or size of same are recited in claim 6. Further, we agree with the Examiner (Ans. 5) that the resultant 6 mm^2 cell area size structure produced by Takashima as modified by Eimori is smaller by a factor of more than 2 than the "no greater than 14 mm^2" cell area claimed, allowing ample room for any required redundant cells.

We further find to be without merit Appellants' argument (Reply Br. 3) that the Examiner's proposed combination of prior art teachings is "a considerable oversimplification of semiconductor process technology." In fact, although Appellants' arguments elaborate on the supposed difficulties in achieving the claimed cell densities, we find ample evidence in the applied prior art to support the Examiner's position that applying known feature size capability (Eimori) to existing $6F^2$ device size teachings (Takashima) will result in a cell density as claimed.

For example, while Appellants contend (App. Br. 11; Reply Br. 5) that factors such as bit line circuitry and bit line spacing affect the feasibility of shrinking a memory cell design to a $6F^2$ size, we find such a contention to be misplaced since Takashima discloses (col. 25, ll. 17-20) that a DRAM memory cell of $6F^2$ size can be achieved. Similarly, while Appellants argue (App. Br. 10-11; Reply Br. 4-5) that shrinkage of a memory cell to a memory cell pitch of less than 1 μm involves significant problems, Eimori discloses (Figure 6) that a memory cell array with a pitch of less than 1 μm has also been achieved.

With the above discussion in mind, we find the Examiner's proffered combination of Takashima, Eimori, Nakamura, and Takahashi reasonably teaches and/or suggests Appellants' claimed invention in terms of familiar

elements that would have been combined by an artisan having common sense using known methods to achieve a predictable result. "The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1161 (Fed. Cir. 2007) (quoting *KSR*, 127 S. Ct. at 1739)).

In view of the above discussion, since the Examiner's prima facie case of obviousness has not been overcome by any convincing arguments from Appellants, we sustain the Examiner's 35 U.S.C. § 103(a) rejection of independent claim 6, as well as dependent claims 7-10 not separately argued by Appellants.

Turning to a consideration of independent claim 18, and its dependent claim 19, based on the combination of Takashima, Eimori, Nakamura, and Takahashi, we sustain the Examiner's obviousness rejection of these claims as well. Claims 18 and 19 differ from previously discussed independent claim 6 in that the claimed cell density is set forth in terms of number of cells, specifically "at least 128," in an area of 100 μm^2. We find no error in the Examiner's analysis (Ans. 4) which concludes that the application of Eimori's 0.25 μm design rule to the $6F^2$ size device of Takashima will result in a density of 270 devices in an area of 100 μm^2. Appellants' arguments reiterate those made with regard to the Examiner's rejection of independent claim 6 attacking the Examiner's proposed application of Eimori's design rule to Takashima's $6F^2$ device, which arguments we found to be unpersuasive as discussed *supra.*

Lastly, we also sustain the Examiner's obviousness rejection, based on the combination of Takashima, Eimori, Nakamura, and Takahshi, of

independent claim 22, as well as dependent claims 23, 25, and 26 not separately argued by Appellants. Appellants' argument (App. Br. 13) in response asserts that, in contrast to the claimed 64M cell integration device, the reference applied by the Examiner to teach a cell integration value, i.e., Nakamura, is a 16M device. Contrary to Appellants' argument, however, as pointed out by the Examiner (Ans. 6), the language of claim 22 requires only that the number of cells be "no more than 68,000,000" cells, a number which is satisfied by Nakamura's disclosure of 16M cell integration.

CONCLUSION

In summary, we have sustained the Examiner's 35 U.S.C. § 103(a) rejections of all of the claims on appeal. Therefore, the decision of the Examiner rejecting claims 6-10, 18, 19, 22, 23, 25, and 26 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv)(2006).

AFFIRMED

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